REMARKS

This responds to the Office Action mailed on March 30, 2005, and the references cited therewith.

Claim 22 is amended. Claims 1-7 and 12-26 remain pending in this application.

Claim Objections

Claim 22 is objected to because of informality. Claim 22 has been amended as requested by the Examiner.

§102 Rejection of the Claims

Claims 12-26 were rejected under 35 U.S.C. § 102(b) for anticipation by Chan et al. (US 4,513,367).

Chan describes a system in which lock bits are used to inhibit replacement or invalidation of cache lines in a processor cache. A special type of command, called a store-interrogate (SI) request, is used to access cache. The SI request sets a lock bit associated with a cache line whether or not the address associated with the request hits or misses in cache. If the request hits in cache, the cache line location is locked. If the request misses in cache, the line in cache where the new cache line will be written is locked in preparation for it being filled with the data read from main memory. When the lock bit is set, its associated cache line cannot be replaced or invalidated.

> If a CP(I) store interrogate (SI) command initiated the XI, the command is immediately searched in each CD(R) [remote copy directory]. If a readonly conflict is detected in the CD(R), the SC having the conflicting CD(R) issues an invalidate (INV) command to its associated PD(R) to invalidate the conflicting line, since the L bit must be off for a line held RO. Then the PD(R) sends an ILE (invalidate line entry) command to the CD(R) to invalidate the line, which is communicated immediately back to CP(I).
>
> If an exclusive (EX) conflict is detected, the CD(R) issues a castout (CO) command to its PD(R). Then PD(R) tests its L bit; and if the L bit is off, PD(R) response to the SC command immediately. But if the L bit is on, PD(R) issues a checkpoint request to its IE(R), does not then castout the line, and does not then

respond to its SC. The issuing CP(I) then must wait until after the checkpoint (which was requested of IE(R)) before CP(I) can receive the requested data. When the requested checkpoint is shortly thereafter provided by IE(R), then PD(R) responds to SC(R) by issuing a CO (castout) command because the line is held EX and was changed. The PD(R) response to SC(R) is communicated to CP(I) for the XI.

If a readonly (RO) conflict is detected, the CD(R) issues an invalidate (INV) command to its PD(R), which must have the L bit off for this RO case. Then PD(R) responds with an ILE command to invalidate the conflicting entry in SIC(R).

If an I/O channel or service processor (SVP) initiates a fetch or store request to main storage, each CD(R) must likewise be cross-interrogated for the address of the request to determine if any SIC has conflicting data. If a conflict is found with a locked line in PD(R), the operations in PD(R) are the same as described for a CP request.

However, if a SVP or I/O channel fetch request finds a conflicting line in CD(R) held RO (a RO line cannot be locked), then a different action is taken, which causes the line to be retained by the associated SIC, and no communication is done with the associated PD(R), and therefore no L bit is tested since no castout or invalidation is required.

To assure the integrity of the XI operation, all copy directories in the MP are searched simultaneously. Therefore, all CD(R)s in the MP are examined for a line address which matches the line address from each CP(I) miss request in the MP. Each CD search operation also detects the presence of any match in all synonym locations for the requested line in every CD. If no match is found in any CD during the search operation, the line fetch request due to the cache miss is immediately accessed in MS. If a match is detected for a synonym in CD(I), the line fetch request is cancelled and the IE access is made in the synonym location in SIC(I). If a match is detected for either the requested address or a synonym address in CD(R), its L bit is tested in PD(R), as previously described.

Col. 13, line 33 – col. 14, line 22.

Chan does teach a form of cache-invalidate instruction, but it relates more to cache coherency than to resource synchronization. However, there is no teaching in Chan of "an instruction that enables the cache-invalidate function to be performed on one or more cache lines of the first cache upon execution of the resource-synchronization instruction." Instead, as noted at col. 8, lines 41-44, "the occurrence of the next checkpoint ends the current checkpoint interval

and resets all L bits. The IE determines when it will issue its next checkpoint signal to that BCE to unlock all locked lines." That is, the instruction can lock the bits, but only the occurrence of a checkpoint interval will unlock the lock bits.

Since a limitation of each of claims 12-26 is not taught in Chan, claims 12-26 do distinguish over Chan. Reconsideration of claims 12-26 is respectfully requested.

Allowable Subject Matter

Claims 1-7 have been found allowable.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date August 30, 2005

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 30th day of August, 2005.

CANDIS BUENDING

Name

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